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**Section 11 - Pulse Width Modulator**

1. On Page 11-4, the description of Bit 0-2 in PWM Control Register should read as:

```
000 = Divide by 4     001 = Divide by 8       010 = Divide by 16
011 = Divide by 32    100 = Divide by 64      101 = Divide by 128
110 = Divide by 256   111 = Divide by 512
```

**Section 12 - Pin Assignment**

1. On Page 12-1, PIn 119 should read as $\overline{\text{LDS}}$/PC2.

2. On Page 12-1, PIn 28 should read as VCC/HiZ.

3. On Page 12-2, the dimensions for G will only have the millimeters (0.5 BSC.). Please discard the inches description (0.20 BSC.).

**Section 13 - Electrical Characteristics- Preliminary**

1. On Page 13-1, Section 13.2, Power Consumption, standby current is 10uA Typical and 20 uA Max at 3.3 volts VDD.



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.....As with other ports, each bit can be individually configured, as needed. *However, PG7_RTCO becomes a dedicated input for 32.768 kHz when PC0_MOCLK is high.* The programmer's model for port G is shown....

4. On Page 7-10, Figure 7-19, the Reset Value for Port G Select Register should be $FFFF.

5. On Page 7-13, Figure 7-23, the Reset Value for Port K Select Register should be $3F3F.

4. On Page 7-14, Figure 7-25, the Reset Value for Port M Select Register should be $FF02.

**Section 8 - UART**

1. On Page 8-12, Figure 8-6, Bits 2 and 3 are now used to control polarity of TXD & RXD and called RXPOL and TXPOL.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RSVD | CLK SRC | Force PERR | LOOP | RSVD | RSVD | RSVD | RSVD | RTS CONT | RTS | IRDA Enable | IRDA Loop | RXPOL | TXPOL | Unused | Unused |

RXPOL 0=Normal 1=Inverted

TXPOL 0=Normal 1=Inverted

**Section 9 - SPI - Slave**

1. On Page 9-3, description of SPI Slave Register bit 15, SPISIRQ, should read:

This interrupt flag bit is asserted at the end of an 8-bit transfer. The data buffer should be read before the completion of another 8-bit transfer. *This bit is cleared by writing a one to it.*

**Section 10 - SPI - Master**

1. On Page 10-3, Figure 10-3, Bit 9 should read as SPIMEN.

2. On Page 10-3, description of Bit 9 of SPIM Control/Status Register should read as:

This bit enables the SPIM. The enable should be asserted before initiating an exchange and should be negated after the exchange is complete. *This bit must be set before data can be written into data register.*

3. On Page 10-4, the description of Bit 8, XCH, should read as:

This bit triggers the state machine to generate (n=clock count) clocks at the selected bit rate. After the n-bit transfer, new data may be loaded and another exchange initiated. At least 2 SPI clocks should elapse before re-enabling this bit. *This bit remains set until the transfer is completed*.

4. On Page 10-4, the description of Bit 7, SPIMIRQ, should read as:

An interrupt is asserted at the end of an exchange (assuming IRQEN is enabled). This bit is asserted until users clear it by writing a 0. Users can write these bits to generate an IRQ on demand. *This bit can also be polled with IRQEN bit clear.*



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**Section 5 - Real-Time Clock**

1. On Page 5-4, Bit 1 and 2 of the Interrupt Status Register (RTCISR) should read as Alarm and MIN Flag, which is shown below:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Unused | | | | | | | | 1 Hz Flag | Day Flag | Alarm Flag | MIN Flag | SW Flag |

**Section 6 - Timer**

1. On Page 6-3, Section 6.2, the first sentence of the second paragraph that begins “Once started,...” should begin, “When enabled,...”.

2. On Page 6-3, Section 6.2, the first two sentences of the fourth paragraph should be deleted and replaced with the following:

> The watchdog timer enable bit is set (register WCR bit WDEN=1)by default at reset activating the watchdog timer. To prevent a reset from occurring, the WDEN bit must be cleared or the counter must be periodically written to prevent the counter from reaching the value of the reference register.

3. On Page 6-3, Section 6.2, the fifth paragraph that reads “The reset source bits.... “ should be deleted.

4. On Page 6-5, for Timer Control Register Bits 3-1, when the value is 1xx, the CLKSOURCE should read 32 kHz or 38 kHz.

5. On Page 6-7, Section 6.4.2.1, the first sentence of the COMPARE VALUE description should read:

> When the counter counts up to the value in this register, an internal MC68328 reset is generated.

6. On Page 6-7, Section 6.4.2.3, Watchdog-Control/Status Register (WCR), the LOCK status bit should be deleted, the W/DRST bit moved to bit 2, and Bits 3 through 15 should be unused as shown below:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Unused | | | | | | | | W/ DRST | FI | WDEN |

7. On Page 6-7, Section 6.4.2.3, Watchdog-Control/Status Register (WCR), the WCR is enabled when reset. Therefore, the reset value for this register is $0001.

8. On Page 6-8, Section 6.4.2.3, Delete LOCK and the description.

**Section 7- Parallel Ports**

1. On Page 7-2, Section 7.1.1.2 Pullup Port, in addition to Port M, Port E, F, G, K are also pullup ports.

2. On Page 7-6, Figure 7-11, the Reset Value for Port D Pullup Register should be $FF00.

3. On Page 7-10, Section 7.1.8 Port G, the description will need to be inserted as follows with the italics:



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2. On Page 4-2, Figure 4-1, System Clock should change to DMA clock, While LCD clock should change to PIXCLK.

3. On Page 4-2, the last paragraph refers to FRC offset register (FOSR), which should be Frame Rate Modulation Control Register (FRCM).

4. On Page 4-7, Section 4.5, the last sentence should read as:

> The MC68328 processor 4-bit LCD interface will drive up to *1024* rows with a maximum of *512* columns.

5. On Page 4-10, Section 4.5.8, the last paragraph should read as:

> When the LCDON bit (register CKCON bit 7) is written to 0, the LCDC enters a low-power mode by stopping it's pixel clock prior to the next line-buffer-fill DMA. In this mode, additional screen DMA and display-refresh operations are stopped. System software should ensure that the PANEL_OFF signal is de-asserted before writing LCDON to 0. When the LCDC is switched back on,(LCDON set to 1) DMA and screen-refresh activities will resume in a synchronous fashion.

6. On Page 4-14, Figure 4-11, the YMAX register uses bits 0-8, with bits 9-15 unused as shown below:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unused | | | | | | | YM8 | YM7 | YM6 | YM5 | YM4 | YM3 | YM2 | YM1 | YM0 |

7. On Page 4-16, The last line of the GS bit description should read as:

> 0 = No gray scale

8. On Page 4-17, Figure 4-20, Bits 5,4,3,2 of the CKCON register should read as WS3,WS2,WS1,WS0.

9. On Page 4-17, Figure 4-20, The Reset Value for the CKCON register should be $40.

10. On Page 4-18, WS1-WS0 should be WS3-WS0. Bits 5,4,3,2 of the CKCON register are used for DMA bursting clock control. Instead of a maximum 4 clock cycle transfer, the LCD controller now supports up to a 16 clock cycle transfer.

```
0000 = 1 clock cycle transfer     1000 = 9 clock cycle transfer
0001 = 2 clock cycle transfer     1001 = 10 clock cycle transfer
0010 = 3 clock cycle transfer     1010 = 11 clock cycle transfer
0011 = 4 clock cycle transfer     1011 = 12 clock cycle transfer
0100 = 5 clock cycle transfer     1100 = 13 clock cycle transfer
0101 = 6 clock cycle transfer     1101 = 14 clock cycle transfer
0110 = 7 clock cycle transfer     1110 = 15 clock cycle transfer
0111 = 8 clock cycle transfer     1111 = 16 clock cycle transfer
```

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**Section 2 - System Integration Module**

1. On Page 2-8, Figure 2-5, the figure title should be ‘‘Interrupt Vector Register.’’

2. On Page 2-9, Interrupt Control Register (ICR) bits for IRQ Edge Trigger Select and Polarity Control are reversed. Bits 15-12 should be POL1 to POL6. Bits 11-8 should be ET1-ET6.

3. On Page 2-11, the RESERVED bit (Bit 5) should be placed between the description of the MRTC bit (Bit 4) and the MKB bit (Bit 6).

4. On Page 2-13, Section 2.3.2.5, the bit order for the Interrupt Wakeup Enable Register (IWR) corresponds to the correct ordering for the IMR Register mentioned in item 3 (Bit 5 is also reserved).

5. On Page 2-14, Figure 2-7, Bit 5 of Interrupt Status Register (ISR) should be Reserved instead of LCDC.

6. On Page 2-16, Figure 2-8, Bit 5 of Interrupt Pending Register (IPR) should be Reserved instead of LCDC.

**Section 3 - Phase-Locked Loop and Power Control**

1. On Page 3-1, Section 3.1, the first paragraph should read as:

> The PLL is a flexible clock source for the MC68328. It provides a crystal-controlled master clock at frequencies from 13 MHz to the maximum operational frequency in 32 KHz steps. The master clock can be divided to provide a system clock as low as 1/16th of the master clock frequency. For the default master clock frequency of 16.58 MHz, the slowest system clock frequency is 1.0363 MHz.

2. On Page 3-1, Figure 3-1, there should be an extra arrow from the block Phase Locked Loop as the DMACLK for the LCD controller.

3. On Page 3-2, Figure 3-2, the address for PLL Control Register should be $(FF)FFF200.

4. On Page 3-5, the example instruction sequence for shutting down the PLL should be:

```
                lea   #$FFF202,A1       ;point to the Freq Sel Register
                lea   #$FFF202,A0       ;
      WAIT      move.w(A0),D0           ;synchronize to rising CLK32 edge
                bpl.w WAIT              ;wait for CLK32 to go high
                bset  #$3,(A1)          ;disable the PLL
                STOP  #$2000            ;stop fetching and wait for any IRQ
   *The system waits here for the PLL to restart after a wakeup IRQ
   * After the IRQ routine, the instruction flow continues from here
                JMP   STARTUP           ;jump to housekeeping routine
```

5. On Page 3-6, Figure 3-4, the arrow pointed to Burst Width Control should be SYSCLK instead of CLK32.

**Section 4 - LCD Controller**

1. On Page 4-1, Section 4.1.2, the last sentence should read as:

> The number of DMA clock cycles per transfer is programmable (1 up to 16 clocks/ transfer), allowing versatile support of systems with varied memory speed requirements.



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### LFLM—First Line Marker

This signal indicates the start of a new display frame. LFLM becomes active after the first line pulse of the frame and remains active until the next line pulse, at which point it de-asserts and remains inactive until the next frame. LFLM can be programmed to be an active-high or an active-low signal.

### LP—Line Pulse

This signal latches a line of shifted data onto the LCD panel. It becomes active when a line of pixel data is clocked into LCD panels and remains asserted for 8 pixel clock periods. LP can be programmed to be either an active-high or an active-low signal.

### LCLK—Shift Clock

This is the clock output to which the output data to the LCD panel is synchronized. LCLK can be programmed to be either an active-high or an active-low signal.

### LACD—Alternate Crystal Direction

This output is toggled to alternate the crystal polarization on the panel. This signal can be programmed to toggle at a period of 1 to 16 frames.

## 18. JTAG TESTING PINS

### TCK—Test Clock

This input provides a clock for onboard test logic defined by the IEEE1149.1 standard.

### TMS—Test Mode Select

This input controls test-mode operations for onboard test logic defined by the IEEE 1149.1 standard. If JTAG is not used, this pin should be connected to Vdd.

### TDI—Test Data In

This input is used for serial test instructions and test data for onboard test logic defined by the IEEE 1149.1 standard.

### TDO—Test Data Out

This output is used for serial test instructions and test data for on-chip test logic defined by the IEEE 1149.1 standard.

### $\overline{\text{JTAGRST}}$—JTAG Reset Input

This input is used for resetting the JTAG module for on-chip test logic defined by the IEEE 1149.1 standard. In normal operation, this pin should be connected to $\overline{\text{RESET}}$.

## USER MANUAL ERRATA

The following information constitutes the errata for the MC68328 DragonBall™ Integrated Processor User's Manual (MC68328UM/AD). The following pages have been amended.

**Section 1 - OVERVIEW**

1. On Page 1-1, The feature described as ''Dynamic Bus Sizing'' should be ''Selectable Bus Sizing.''

2. On Page 1-12, Table 1-3, the name for address Base+$61A should be ''WRR.''



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## 14. TIMER PINS

### PG6/TIN1—Timer 1 Input, Port G 6

This bidirectional pin can be programmed as a clock input that causes events to occur in timer/counter channel 1, either causing a clock to the event counter or providing a trigger to the timer value capture logic. By default after reset, this pin becomes general-purpose input, PG6.

### PG4/TIN2—Timer 2 Input, Port G 4

This bidirectional signal can be programmed as a clock input that causes events to occur in timer/counter channel 2, either causing a clock to the event counter or providing a trigger to the timer value capture logic. By default after reset, this pin becomes general-purpose input, PG4.

### PG5/TOUT1 —Timer 1 Output, Port G 5

This bidirectional signal can be programmed to toggle or generate a pulse of one system clock duration when timer/counter channel 1 reaches a reference value. By default after reset, this pin becomes general-purpose input, PG5.

### PG3/TOUT2 —Timer 2 Output, Port G 3

This bidirectional signal can be programmed to toggle or generate a pulse of one system clock duration when timer/counter channel 2 reaches a reference value. By default after reset, this pin becomes general-purpose input, PG3.

## 15. PWM PIN

### PG2/PWMO—Pulse Width Modulator Output, Port G 2

This pin can serve as the PWM output signal. When it is PWMOUT, it produces synthesized sound, which can be connected to an audio amplifier and filter to generate melody and tone. By default after reset, this pin becomes general-purpose input, PG2.

## 16. RTC PINS

### PG7/RTCO—Real-Time Clock Output/Input, Port G 7

While PC0/MOCLK is high, this pin is a dedicated input that provides the 32.768 kHz or 38.4 kHz clock to the real-time clock. While PC0/MOCLK is low, this pin can be programmed to output constant time tick pulses at the crystal frequency. By default after reset while PC0/MOCLK is low, this pin becomes general-purpose input, PG7.

## 17. LCD CONTROLLER PINS

### LD3-LD0—LCD Data Bus

This output bus transfers pixel data to the LCD panel for display. The pixel data is arranged to accommodate the programmable panel mode data width selection. Panel interfaces of one, two, or four bits are supported. Users can also program the output pixel data to be inverted for those LCD panels that require it.

The MC68328 LCD interface data bus uses LD0 to display pixel 0, 0. Some LCD panel manufacturers specify their LCD panel data bus where data bit 3 of the panel displays pixel 0,0. For these panels, the connections from the MC68328 LD bus to the LCD panel data bus are reversed in bit significance. Therefore, for these panels, connect LD0 of the MC68328 to LCD panel data bit 3, LD1 to LCD data 2, LD2 to LCD data 1, and LD3 to LCD data 0.



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### PK2/SPMCLK—Master SPI Clock, Port K 2

This pin is the clock output when the SPIM is enabled. In polarity = 0 mode, this signal is low while the SPIM is idle. In polarity = 1 mode, this signal is high during idle. By default after reset, this pin becomes general-purpose input, PK2.

## 12. SLAVE SPI PINS

### PK5/SPSCLK—Slave SPI Clock, Port K 5

This pin is the slave SPI clock output. By default after reset, this pin becomes general-purpose input, PK5.

### PK4/SPSRXD-Slave SPI Receive Data, Port K 4

This pin is the slave SPI shift register input. By default after reset, this pin becomes general-purpose input, PK4.

### PK3/SPSSEN-Slave SPI Enable, Port K 3

This pin is the slave SPI enable. While this signal is active, 8 clocks shift data into the slave SPI. This bit is programmable to be active high or low. By default after reset, it becomes general-purpose input, PK3.

## 13. UART PINS

### PG0/TXD—UART Transmit Data, Port G 0

This pin is the transmitter serial output. While in normal mode, NRZ data is output. While in IrDA mode, a 3/16 bit-period pulse is output for each “zero” bit transmitted. For RS-232 applications, this pin must be connected to an RS-232 transmitter. For infrared applications, this pin can directly drive an IR LED. By default after reset, this pin becomes general-purpose input, PG0.

### PG1/RXD—UART Receive Data, Port G 1

This pin is the receiver serial input. While in normal operation, NRZ data is expected. While in infrared mode, a narrow pulse is expected for each “zero” bit received. External circuitry must be used to convert the infrared signal to an electrical signal. RS-232 applications need an external RS-232 receiver to convert voltage levels. By default after reset, this pin becomes general-purpose input, PG1.

### PM0/$\overline{\text{CTS}}$—Clear to Send, Port M 0

This input controls the transmitter. Normally, the transmitter waits until this signal is active (low) before a character is transmitted. If the IGNORE CTS bit is set, the transmitter sends a character whenever a character is ready to transmit. This pin can then be used as a general-purpose input whose status is read in the CTS STATUS bit. This pin can post an interrupt on any transition of $\overline{\text{CTS}}$, if enabled. By default after reset, this pin becomes $\overline{\text{CTS}}$.

### PM1/$\overline{\text{RTS}}$—Request to Send, Port M 1

This pin serves two purposes. Normally, the receiver indicates that it is ready to receive data by asserting this pin (low). This pin would be connected to the far-end transmitter’s $\overline{\text{CTS}}$ pin. When the receiver detects a pending overrun, it negates this pin. For other applications, this pin can be a general-purpose output controlled by the bit in the receiver register. When it is programmed as parallel I/O, it becomes PM1. By default after reset, this pin becomes general-purpose input, PM1.

### PM7/GPIO—UART General Purpose I/O, Port M 7

This pin provides several functions for the UART. It can provide a bit clock (input or output) and a master clock for the baud generator (input). By default after reset, this pin becomes UART GPIO.



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any one key of the row lines is pressed, an interrupt is generated to signal to the CPU to scan the keys. This feature, together with the pen interrupt, contributes a significant portion of the power management activities.

### PM6/$\overline{\text{PENIRQ}}$—Pen Interrupt Input And General-Purpose I/O

Users can program this pin as a general-purpose I/O PM6 or pen-interrupt input. When programmed as a pen-interrupt signal, this pin accepts an active low, level-triggered interrupt from the pen input device for a “pen-down” action.

### PM5-PM2/$\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ6}}$

These pins can be programmed to either parallel I/O PM2-PM5 or interrupt input. When they function as interrupt inputs, they can be programmed to be edge or level triggered with either high or low polarity. $\overline{\text{IRQ6}}$ generates a level 6 interrupt $\overline{\text{IRQ3}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$ generated level 3, 2 and 1 interrupts respectively.

## 9. CHIP SELECT PINS

### CSA0—Boot Chip-Select

$\overline{\text{CSA0}}$ is the default chip-select after reset. It is set to 6 wait states and decodes all address ranges except internal register address space. It can be reprogrammed during the boot sequence to another address range and different wait states.

### $\overline{\text{PE7-PE1/CSB3-CSB0}}$, $\overline{\text{CSA3-CSA1}}$—Chip-Select Group A and B

These pins comprise the remainder of the Group A and Group B chip-selects and are individually programmable. Pins that are not needed as chip-selects can be programmed as general-purpose I/Os. By default after reset, $\overline{\text{CSB3}}$ is disabled and functions as a general-purpose input.

### PJ7-PJ0/$\overline{\text{CSD3-CSD0/CSC3-CSC0}}$—Chip-Select Group C and D

These pins comprise the Group C and Group D chip-selects and are individually programmable. Pins that are not needed as chip-selects can be programmed as general-purpose I/Os.

## 10. PCMCIA 1.0 PINS

### PC6/$\overline{\text{WE}}$—Write Enable, PC6

This pin can be programmed as either a PC6 parallel I/O or a write-enable signal for the PCMCIA 1.0 card interface. The MC68328 processor drives the active-low $\overline{\text{WE}}$ signal to indicate a memory-write transfer to the PCMCIA 1.0 card**.** When programmed as I/O, it serves as PC6.

### PK7-PK6/$\overline{\text{CE1}}$-$\overline{\text{CE2}}$

These pins can be programmed as either parallel I/O port K 7-6 or the PCMCIA 1.0 chip-enable signal. When programmed as the PCMCIA chip-enable, the $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ lines are active-low, card-enable signals driven by the MC68328 processor; $\overline{\text{CE1}}$ enables even bytes; $\overline{\text{CE2}}$ enables odd bytes. $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are decoded for assertion by $\overline{\text{CSD3}}$.

## 11. MASTER SPI PINS

### PK0/SPMTXD—Master SPI Transmit Data, Port K 0

This pin is the master SPI shift register output. By default after reset, this pin becomes general-purpose input, PK0.

### PK1/SPMRXD—Master SPI Receive Data, Port K 1

This pin is the input to the master SPI shift register. By default after reset, this pin becomes general-purpose input, PK1.



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### PB7-PB0/D7-D0

This bus is the lower data byte or general-purpose I/O. In pure 8-bit systems, this bus can serve as a general-purpose I/O. The WDTH8 bit in the system control register ($FFF000) should be set to one (1) by software before the port can be used. In 16-bit or mixed 8-/16-bit systems, these pins must function as the lower data byte.

## 7. BUS CONTROL PINS

### $\overline{\text{AS}}$—Address Strobe

This active-low output signal indicates that a valid address is present on the address bus. It is not asserted during LCD DMA accesses.

### R/$\overline{\text{W}}$—Read/Write

This output signal defines the data bus transfer as a read or write cycle; read = 1; write = 0.

### PC1/$\overline{\text{UDS}}$—Upper Data Strobe/Port C I/O

This pin can be programmed as $\overline{\text{UDS}}$ or as a general-purpose I/O. When used as upper data strobe ($\overline{\text{UDS}}$) output, this active-low signal is asserted when the internal EC000 core does a 16-bit word access or an even byte access.

### PC2/$\overline{\text{LDS}}$—Lower Data Strobe/Port C I/O

This pin can be programmed as $\overline{\text{LDS}}$ or as a general-purpose I/O. When used as lower data strobe ($\overline{\text{LDS}}$) output, this active-low signal is asserted when the internal EC000 core does a 16-bit word access or an odd byte access.

### $\overline{\text{LWE}}$, $\overline{\text{UWE}}$ — Lower Byte Write-Enable and Upper Byte Write-Enable

On a write cycle to a 16-bit port, these active-low output signals indicate when the upper or lower 8 bits of the data bus contain valid data. In 8-bit mode or when the BSW bit in the chip-select register is 0, use only the upper write-enable ($\overline{\text{UWE}}$) for write-enable control.

### PC4/$\overline{\text{IRQ7}}$—Level 7 Interrupt/Port C I/O

When programmed as peripherals, this signal is an active-low input which, when asserted, will generate a level 7 interrupt to the CPU. When programmed as I/O, it becomes the PC 4 parallel I/O port.

### PC5/$\overline{\text{DTACK}}$—Data Transfer Acknowledge, PC5

This pin can be programmed as parallel I/O PC5 or $\overline{\text{DTACK}}$. While programmed as $\overline{\text{DTACK}}$, this input signal indicates that the data transfer has been completed. $\overline{\text{DTACK}}$ is normally generated internally for all chip-selects. For systems that address spaces outside of the chip-select ranges, $\overline{\text{DTACK}}$ must be generated externally.

### $\overline{\text{OE}}$—Output-Enable

This active-low signal is asserted during a read cycle of the MC68328 processor, which enables the output of either ROM or SRAM. This signal also serves the PCMCIA 1.0 interface to indicate a read cycle.

## 8. INTERRUPT CONTROL PINS

### PD0-PD7/$\overline{\text{KB0}}$-$\overline{\text{KB7}}$/$\overline{\text{INT0}}$-$\overline{\text{INT7}}$—Keyboard and General-Purpose Interrupt Lines

Users can program these signals as interrupt inputs or parallel I/O ports. For an interrupt port application, $\overline{\text{INT0}}$-$\overline{\text{INT7}}$ can be configured to perform keyboard interrupt functions. Keyboard interrupt pins $\overline{\text{KB0}}$-$\overline{\text{KB7}}$ are pulled high internally and connected to the rows of the keyboard matrix with the column driven low. When



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### CLKO—Clock Out

This output clock signal is derived from the on-chip clock oscillator and is internally connected to the clock output of the internal PLL. This signal is provided for external reference. The output can be disabled to reduce power consumption.

### PC0/MOCLK—Clock Mode Select, Port C I/O

While this pin is high, the MC68328 processor is in the external clock mode and the on-chip PLL is disabled. The system clock must be driven into the EXTAL pin. While this pin is low, it enables the PLL. Either a 32.768 kHz or 38.4 kHz clock can be driven in to the EXTAL pin, or a crystal can be connected between EXTAL and XTAL to create an oscillator. PC0/MOCLK can be programmed as a general-purpose I/O while the internal PLL is enabled.

## 5. SYSTEM CONTROL

### $\overline{\text{RESET}}$

This active-low input signal causes the entire MC68328 processor (CPU and peripherals) to enter the reset state (cold reset). Users should drive this signal low for at least 100 msec at initial power-up to ensure that the crystal oscillator starts and stabilizes.

### BBUSW—Boot Bus Width-Select

This input defines the data bus width for the boot chip-select, $\overline{\text{CSA0}}$. BBUSW = 0 means the boot chip-select addresses an 8-bit memory space. BBUSW=1 means the boot memory space is 16-bits wide. Users can create a mixed 8/16 bit memory system by programming the memory space widths in the various chip-select control registers.

## 6. ADDRESS BUS PINS (A31–A0)

These are the address lines driven by the 68EC000 core or by the LCD controller for panel refresh DMA. The chip-select module can decode the entire 4 Gbyte address map. In many applications, only the lower portion of the address lines will be used, reserving any unused address pins for parallel I/O functions.

### A15—A0

These address output lines are not multiplexed with any other I/O signals.

### PA7-PA0/A16-A23

These address lines are multiplexed with I/O port A. When programmed as I/O ports, they serve as general-purpose I/O ports; otherwise, they are output-only address signals. These signals default to address lines at reset where the address lines are all zeroes. Users should note that there may be contention if any logic “1” levels are driving these pins after reset.

### PF7-PF0/A31-A24

These bus pins are the extended address for 68EC000 core and are multiplexed with port F. In most systems, these lines are not used as addresses because most memory chips can be mapped into blocks of less than 16 Mbytes. These pins default to the port F I/O function after reset.

### Data Bus Pins (D15—D0)

The flexible data bus interface design of the MC68328 processor allows users to program the lower byte of the data bus in an 8-bit-only system as general-purpose I/O signals.

### D15-D8

The upper byte of the data bus is not multiplexed with any other signals. In pure 8-bit systems, this is the data bus. In mixed 8-/16-bit systems, 8-bit memory blocks or peripherals should be connected to this bus.



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**Table 1. Signal Definitions (Continued)**

| | | |
|---|---|---|
| Interrupt Control/PDIO/ Keyboard Interrupt | PD7-PD0/$\overline{KB7}$-$\overline{KB0}$/$\overline{INT7}$-$\overline{INT0}$ | 8 |
| Interrupt Control/PMIO | $\overline{PM5}$/$\overline{IRQ1}$, $\overline{PM4}$/$\overline{IRQ2}$, PM3/$\overline{IRQ3}$, PM2/$\overline{IRQ6}$, PM6/ $\overline{PENIRQ}$, PC4/IRQ7 | 6 |
| LCD Control | LACD, LCLK, LLP, LFRM, LD0-LD3 | 8 |
| UART/PMIO/PGIO | PM7/GPIO, PG1/RXD, PG0/TXD, PM0/$\overline{CTS}$, PM1/$\overline{RTS}$ | 5 |
| Timer/PGIO | PG4/TIN2, PG6/TIN1, PG3/TOUT2, PG5/TOUT1 | 4 |
| RTC/PGIO | PG7/RTCO | 1 |
| PWM/PGIO | PG2/PWMO | 1 |
| Chip Select | $\overline{CSA3}$–$\overline{CSA0}$, $\overline{CSB0}$-$\overline{CSB3}$, $\overline{CSC0}$-$\overline{CSC3}$, $\overline{CSD0}$-$\overline{CSD3}$ PE7-PE0, PJ7-PJ0 | 16 |
| IEEE Testing | TMS, $\overline{JTAGRST}$, TDI, TDO, TCK | 5 |
| Power | $V_{DD}$, $PLLV_{DD}$ | 10 |
| Ground | $V_{SS}$, $PLLV_{SS}$ | 10 |

**NOTE**

All pins except EXTAL support TTL levels. EXTAL, when used as an input clock, needs a CMOS level. To ensure proper low-power operation, all inputs should be driven CMOS level. Using a TTL level to drive those inputs could result in higher power consumption.

## 3. POWER PINS

The MC68328 processor has 20 power supply pins. Users should be careful to reduce noise, potential crosstalk, and RF radiation from the output drivers. Inputs may be +5 V or +3.3V when $V_{DD}$ = +3.3V or +5V respectively without damaging the device.

- $V_{DD}$ (9)—9 power pins
- $V_{SS}$ (9)—9 ground pins
- $PLLV_{DD}$ (1)—1 power pin for the PLL
- $PLLV_{SS}$ (1)—1 ground pin for the PLL

## 4. CLOCKS

### EXTAL—External Clock/Crystal Input

This input provides 3 clock generation options: (1) low frequency crystal, (2) low frequency external clock, and (3) high frequency external clock. While PC0/MOCLK is low, the on-chip phase-locked loop is enabled, creating the high-speed system clock from a low frequency reference. EXTAL may be used (with XTAL) to connect an external crystal to the on-chip oscillator and clock generator. If an external clock instead of a crystal is used, the clock source should be connected to EXTAL, and XTAL left unconnected. The internal PLL generates the system clock at 16.58 MHz from a 32.768 kHz or 38.4 kHz source. When an external clock is used, it must provide a CMOS level at this input frequency.

While PC0/MOCLK is high, the PLL is disabled and the system clock must be connected to the EXTAL pin. If the real-time clock is used, 32.768 kHz or 38.4 kHz must be driven into PG7/RTCO.

### XTAL—Crystal Output

This output connects the on-chip oscillator output to an external crystal. If an external clock is used, XTAL should remain unconnected.



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*Addendum and Errata to*

# MC68328 DragonBall™ Integrated Microprocessor User's Manual

**February 6, 1996**

This addendum to the initial release of the MC68328 User's Manual provides corrections to the original text, plus additional information not included in the original. This document and other information on this product is maintained on the AESOP BBS, which can be reached at (800) 843-3451 (from the U.S. and Canada) or (512) 891-3650. Configure modem for up to 14.4Kbaud, 8 bits, 1 stop bit, and no parity. Terminal software should support VT100 emulation. Internet access is provided by telneting to pirs.aus.sps.mot.com [129.38.233.1] or through the World Wide Web at http://pirs.aus.sps.mot.com.

## 1. SIGNAL DESCRIPTIONS

This addendum describes the MC68328 DragonBall™ integrated microprocessor pinout. The input and output signals of the MC68328 processor are organized into functional groups and are described in the following sections. The MC68328 processor is offered in a 144-lead plastic thin-quad flat package (TQFP).

The MC68328 processor uses a standard M68000 bus for communication between both on-chip and external peripherals with optional address extension to A31. This single continuous bus exists both on- and off-chip of the MC68328 processor. Read accesses made by the core to internal memory mapped registers of the device are invisible on the external bus. Write accesses made by the core to internal or external memory mapped locations are visible on the external bus.

## 2. FUNCTIONAL GROUPS

The MC68328 processor group signals are shown in Table 1.

**Table 1. Signal Definitions**

| Functional Group | Signals | Number of Pins |
|---|---|---|
| Clocks/PCIO | XTAL, EXTAL, CLKO, PC0/MOCLK | 4 |
| System Control/PCIO | $\overline{\text{RESET}}$, BBUSW | 2 |
| Address Bus, PAIO | PA7-PA0/A23-A16, A15–A0 | 24 |
| Extended Address Bus/ PFIO | PF7-PF0/A31-A24 | 8 |
| Lower Data Bus/PBIO | PB7-PB0/D7–D0 | 8 |
| Upper Data Bus | D15-D8 | 8 |
| Bus Control/PCIO | PC1/$\overline{\text{UDS}}$, PC2/$\overline{\text{LDS}}$, PC5/$\overline{\text{DTACK}}$, $\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{OE}}$, $\overline{\text{UWE}}$, $\overline{\text{LWE}}$ | 8 |

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